REMARKS

Applicant herewith amends paragraph [0006] in the specification to provide a missing patent reference. A minor typographical error has also been corrected in paragraph [0006]. The amendments are quite self-explanatory.

Applicant takes this opportunity to inform the Examiner that the present application is related to U.S. Application Serial No. 10/339, 752 titled "Method and System for Delay Control in Synchronization Circuits", which was filed on January 8, 2003 and assigned to the assignee of the present application.

Claims 1-50 were submitted for examination. The present response amends claims 16, 19, 39, and 41-50. After the present claim amendments, claims 1-50 still remain pending in the application.

I. Section 112 Rejection

Claims 41 and 46 were rejected under 35 U.S.C. § 112, para. 2, as being indefinite because of the recitation of "one circuit" to refer to two different circuits. Applicant has amended each of the claims 41 and 46 to replace the two occurrences of "one circuit" with "a first circuit" and "a second circuit." Applicant believes that the amendments to claims 41 and 46 clarify the reference to two different circuits, as was correctly understood by the Examiner during examination of the claims. In view of the present amendments to claims 41 and 46, Applicant respectfully requests that the Examiner withdraw the § 112 rejection.

II. Section 102 Rejection

Claims 1-10 and 41-42 were rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,445,231 to Baker et al. (hereafter "Baker"), and claims 11-20, 31-40, and 43-50 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,923,715 to Ono (hereafter "Ono"). Applicants traverse the rejection of claims 1-20 and 31-50 in light of the following remarks and present claim amendments.

A. Non-Anticipation by Baker

As discussed in paragraph [0006] in the present application, Baker teaches a circuit in which the delay line is comprised of both a coarse loop and a fine loop. The coarse loop is designed to produce an output signal having a phase variation from an input signal within a coarse delay stage while the fine loop is designed to produce an output signal having a phase deviation from the input signal which is substantially smaller than the deviation of the coarse loop. The coarse loop is designed to bring the output signal to a near phase lock condition, or phase delayed condition, while the fine loop is designed to achieve a locked condition. Thus, a dual-loop (coarse and fine loops) all digital PLL or DLL can provide a wide lock range while at the same time still providing a tight lock within reasonable time parameters.

The independent claim 1 recites, among other things, "a delay line having a first portion providing a variable amount of delay substantially independently of process, temperature and voltage variations and a second portion in series with said first portion and providing a variable amount of delay that substantially tracks changes in process, temperature, and voltage variations." Although the Examiner has expressly acknowledged on page 21 (item-51) of the Office Action that Baker fails to teach this quoted limitation, the Examiner relies on the inherency doctrine and an incorrect reading of Baker to reject claim 1. Applicant finds no support in the portion of Baker cited by the Examiner in item-6(a) of the Office Action for the Examiner's assertion that Baker teaches the above quoted limitation. In view of the Examiner's own admission of Baker's failure to teach this limitation of claim 1 and in view of Baker's actual failure to teach this limitation, Applicant asserts that claim 1 is not anticipated by Baker.

Claims 2-10 depend from the independent claim 1 and, hence, are also not anticipated by Baker at least for the same reasons given above. Further, the amended independent claim 41 also contains a limitation similar to the one reproduced above with reference to claim 1 and, hence, claim 41 is also not anticipated by Baker.

The amended independent claim 42 recites in part "propagating a signal through two different types of series-connected delay circuits, one circuit having a small intrinsic delay and

the other circuit having a larger intrinsic delay." Applicant asserts that Baker fails to teach such propagation through two series-connected delay circuits with different intrinsic delays. In fact, the Examiner has expressly acknowledged on page 23 (item-56) of the Office Action that Baker does fail to teach this quoted limitation. Still, the Examiner again relies on the inherency doctrine and linking of intrinsic delay with PVT dependence (without citation to any authority or technical literature) to reject claim 42. Applicant finds no support in the portion of Baker cited by the Examiner in item-17(a) of the Office Action for the Examiner's assertion that Baker teaches the above quoted limitation. In view of the Examiner's own admission of Baker's failure to teach this limitation in claim 42 and in view of Baker's actual failure to teach this limitation, Applicant asserts that claim 42 is also not anticipated by Baker.

In view of the arguments given hereinabove, Applicant requests that the Examiner withdraw the § 102(e) rejections of pending claims 1-10 and 41-42. Reconsideration and allowance of claims 1-10 and 41-42 is respectfully requested.

B. Non-Anticipation by Ono

Ono teaches a digital PLL circuit that has a frequency comparator circuit for comparing the frequencies of an output clock signal and a reference clock signal to generate frequency comparator information. A delay control circuit generates a predetermined digital signal based on the frequency comparator information, and a clock signal generating circuit generates the output clock signal of the PLL circuit. The clock signal generating circuit changes the oscillation frequency of the output clock signal in response to the predetermined digital signal generated by the delay control circuit. The number of connected delay stages in a variable delay circuit (of the clock signal generating circuit) is controlled on the basis of the output of the frequency comparator circuit. Additionally, variable load capacitance circuits in the variable delay circuit are controlled mainly on the basis of the output of the frequency comparator. In this way, a digital PLL having small jitter and a high accuracy is provided.

Each of the independent claims 11, 31, 43, and 48 recites, among other things, " a first circuit path" having "a stepwise variable capacitive load" and "a second circuit path in series

with the first circuit path and having a plurality of stages each having at least two paths." (Emphases added.) Applicant asserts that Ono fails to teach such series-connected circuit paths. According to the Examiner, the "first circuit path" is via the load capacitance control unit 12 in Ono (Figures 1-2, Ono) and the "second circuit path" is via the delay stage control unit 13 in Ono. Applicant initially observes that except for the Up/Down counter 88 in Figure 4(c) in Ono, no additional constructional details of the control unit 13 is provided in Ono. That is, no "plurality of stages" with each stage "having at least two paths" is shown for the control unit 13 in Ono.

Applicant respectfully submits that the Office has misconstrued the teachings of Ono. More specifically, it is believed that Ono fails to disclose a second circuit path which includes a "plurality of stages each having at least two paths." In Figure 2, Ono discloses a variable delay circuit (16) which includes a plurality of inverter pairs (23, 24). As seen in Figure 3, the inverters in each inverter pair (23, 24) are serially connected (i.e., each stage has a single path). The output of each inverter pair is connected to an input of a multiplexer (20). Ono states:

> One of the input terminals 0 through 2^{s-1} of the multiplexer 20 is selected based on the value of the delay stage control signals E_{s1} through E_{ss}. Because each input terminal of the multiplexer is connected to the output of one of the 2^s stages of inverters, a selected number of stages of inverters (corresponding to the selected input terminal) are connected to the output of the variable delay circuit to generate a predetermined delay value.

(Column 5, lines 1 – 8.) It is respectfully submitted that regardless of which "one of the input terminals ... of the multiplexer 20 is selected," the resulting "second circuit path" does not include "a plurality of stages" wherein each stage has two paths. For example, referring to Figure 2, if input terminal 0 is selected, the circuit path serially runs from the input, through inverters 21 and 22, through the multiplexer 20 and to the output. If input terminal 1 is selected, the circuit path includes the inverter stage 23 and serially runs from the input, through inverters 21 and 22, through inverter pair 23, through the multiplexer 20, and to the output. As a result, the smallest delay increment that can be achieved by Ono's circuit is equal to two gate delays (i.e., each inverter in the inverter pair has one gate delay).

In contrast, claims 11, 31, 43, and 48 each recite "a second circuit path in series with the first circuit path and having a plurality of stages each having at least two paths." Also, claims 19, 39, 45, and 50 each recite similar "second circuit path", except that each of the claims 19, 39, 45, and 50 specifically recites that the "second circuit path" therein has "a plurality of stages each having at least a fast and a slow path" (i.e., each stage has at least two paths). As discussed in the specification, page 6, paragraph [0027]:

> The embodiment illustrated in FIG. 4 includes a slow path 65 which is comprised of a first inverter 66, a second inverter 67 and a multiplexer 68. A fast path 70 is similarly comprised of a first inverter 71, a second inverter 72, and a multiplexer 73. By varying the size of the inverter in the slow path 65, a different delay resolution can be achieved.

It is respectfully submitted that the claimed combination can achieve a finer delay adjustment than the prior art. Thus, for the reasons discussed above, it is believed that independent claims 11, 19, 31, 39, 43, 45, 48, and 50 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 11, 19, 31, 39, 43, 45, 48, and 50 pursuant to §102(b) in view of Ono be withdrawn.

Claims 12-15 depend from allowable independent claim 11, claims 32-35 depend from allowable independent claim 31, claim 20 depends from the allowable independent claim 19, and claim 40 depends from the allowable independent claim 39. Thus for the same reasons discussed above in conjunction with non-anticipation of claims 11, 19, 31, and 39, it is believed that respective dependent claims 12-15, 20, 32-35, and 40 are also in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 12-15, 20, 32-35, and 40 pursuant to §102(b) in view of Ono be withdrawn.

Each of the independent claims 16, 36, 44, and 49 recites, among other things, " a first circuit path having a stepwise variable capacitive load" and "a second circuit path in series with said first circuit path and having a plurality of stages each having a variable amount of drive associated therewith." (Emphases added.) Applicant asserts that Ono fails to teach such series-connected circuit paths. Applicant notes the Examiner's failure in the Office Action to clearly point out on page 9, item 25(b) in the Office Action how Ono teaches the "second circuit

path...having a plurality of stages each having a variable amount of drive associated therewith." (Emphasis added.) In any event, Applicant asserts that Ono fails to teach that each inverter-multiplexer based "circuit path" in Ono has a "variable amount of drive associated therewith" as required under each of the independent claims 16, 36, 44, and 49.

As discussed in the specification, page 7, paragraph [0034]:

> FIG. 7 illustrates another example of how the fine delay may be adjusted by adjusting the amount of drive. The phase detector 80 produces the FAST and SLOW control signals which are input to a selection control block 88. The selection control block 88 produces signals for controlling individual drive stages 90, 91, 92, 93. One of the drive stages, drive stage 91, is illustrated as a pair of parallel connected inverters, and one of the inverters is illustrated in detail in FIG. 7A. Thus, the selection control block 88 determines if one or both paths within drive stages 90, 91, 92, 93 are used.

The Examiner does not point out how, if at all, such "second circuit path" is discussed or taught in Ono. Further, Applicant also fails to find in Ono any discussion or teaching of variability of drive for each stage in the "second circuit path."

From the discussion above, it is believed that independent claims 16, 36, 44, and 49 are not anticipated by Ono and, hence, are in condition for allowance. Accordingly, it is respectfully requested that the rejection of independent claims 16, 36, 44, and 49 pursuant to §102(b) in view of Ono be withdrawn.

Claims 17-18 depend from allowable independent claim 16 and claims 37-38 depend from allowable independent claim 36. Thus for the same reasons discussed above in conjunction with non-anticipation of claims 16 and 36, it is believed that claims 17-18 and 37-38 are also in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 17-18 and 37-38 pursuant to §102(b) in view of Ono be withdrawn.

The amended independent claim 46 recites in part "propagating said signal through two different types of variable delay circuits, a first circuit being substantially independent of process, temperature and voltage variations and a second circuit tracking changes in process, temperature, and voltage variations." Applicant asserts that Ono fails to teach such propagation.

The Examiner's assertion that such propagation through two different types of variable delay circuits is "inherent" in Ono stems from an incorrect reading of Ono. The Examiner does not cite to any portion in Ono where such PVT-independent and PVT-dependent delay circuits are taught—either expressly or by necessary implication (i.e., "inherently"), although in view of MPEP § 2112 (Eighth Edition incorporating Revision No. 1, 2003), the burden is on the Examiner to provide rationale or evidence tending to show such inherency. The MPEP § 2112 mandates, citing *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999), that:

> To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

Based on the above arguments, Applicant asserts that claim 46 is not anticipated by Ono. Hence, the Applicant requests that the Examiner withdraw the § 102(b) rejection of claim 46 over Ono. Reconsideration and allowance of claim 46 is respectfully requested.

The amended independent claim 47 recites in part "propagating said signal through two different types of delay circuits, one circuit having a small intrinsic delay and the other circuit having a larger intrinsic delay." Applicant asserts that Ono fails to teach such propagation. Similar to the rejection of claim 46, the Examiner also asserts here that such propagation through two different types of delay circuits having different "intrinsic" delays is "inherent" in Ono. As before, the Examiner misreads Ono and does not cite to any portion in Ono where such delay circuits with different "intrinsic" delays are taught—either expressly or by necessary implication (i.e., "inherently"). Because the Examiner fails to satisfy his burden of establishing inherency as required under MPEP § 2112 (portions of which are cited hereinabove with reference to discussion of non-anticipation of claim 46), Applicant asserts that claim 47 is not anticipated by Ono. Hence, Applicant requests that the Examiner withdraw the § 102(b) rejection of claim 47 over Ono. Reconsideration and allowance of claim 47 is respectfully requested.

In view of the arguments given hereinabove, Applicant requests that the Examiner withdraw the § 102(b) rejections of pending claims 11-18, 31-38, 43-44, and 46-49.

III. Section 103 Rejection

Claims 21-30 were rejected under 35 U.S.C. § 103(a) as being obvious over Baker in view of U.S. Patent No. 5,808,478 to Andresen (hereafter "Andresen"). Applicant traverses the rejection of claims 21-30 in view of the following remarks.

Andresen is directed to an output buffer with a slew rate that is load independent. The output buffer is controlled such that it can drive a load with different drive levels by changing the transconductance internal thereto. A delay block introduces an amount of delay tracking the overall intrinsic delay associated with the output buffer. The intrinsic delay changes with temperature, voltage, and process variations. A variable delay block selectively introduces a determined amount of delay into the delay path which does not vary with process, voltage, and temperature conditions. After these delay blocks, a window comparator compares the actual output voltage level with the desired voltage level to determine the difference therebetween. A control system generates the drive control signal at a value to vary the drive level of the output buffer to reduce the difference between the actual and desired voltage levels.

In rejecting independent claim 21, the Examiner acknowledges Baker's failure to teach a "chain of delay circuits wherein the first is independent of PVT variation and the second is dependent on PVT variation." (Office Action, page 21, item 51.) However, the Examiner relies on Andresen to supply this missing limitation. Assuming, *arguendo*, that combining the teachings of Baker with the teachings of Andresen is proper, that combination still fails to teach or suggest all limitations recited in the independent claim 21. For example, as per the Examiner's observation, even if the variable delay 40 and the intrinsic delay 38 in Andresen's buffer 10 (Andresen, Figs. 1-2) are considered the "first portion" and the "second portion", respectively, of the "delay line" element recited in claim 21, there is still no teaching or suggestion in Andresen of "a control circuit for controlling the delay of said delay line [which includes the first and the second portions]" as recited in claim 21. Nor does Baker teach or suggest such "control circuit" in combination with the "phase detector," the "feedback path," and other elements recited in claim 21. The so-called "delay line" of Andresen (which, according to the Examiner, includes the units 38 and 40 in Fig. 2 in Andresen) is in fact used to generate control signals for the output

buffer 14 in Andresen and is not itself controlled by "a control circuit" as required under claim 21. The discussion at columns 3 and 4 in Andresen supports this observation.

Further, even though the Examiner finds Andresen combinable with Baker to reject claim 21, Applicant respectfully disagrees with that finding. Applicant observes that the Examiner doesn't point to any portion in Andresen where the desirability of combining the teachings of Andresen (e.g., output buffer 10 (Andresen, Figure 1)) with the teachings of Baker (e.g., a delay locked loop design) is taught or suggested.

Based on the foregoing discussion, Applicant asserts that the combined teachings of Baker and Andresen fail to teach or suggest all claim limitations recited in independent claim 21 and, hence, fail to render claim 21 obvious under 35 U.S.C. § 103(a). Reconsideration and allowance of claim 21 is therefore respectfully requested.

Claims 22-25 are dependent on allowable independent claim 21 and, hence, are also not rendered obvious by the combined teachings of Baker and Andresen. Therefore, reconsideration and allowance of claims 22-25 is respectfully requested.

In rejecting independent claim 26, the Examiner acknowledges Baker's failure to teach a "chain of delay with a first portion with smaller and, a second portion with larger intrinsic delay value." (Office Action, pages 23-24, item 56.) However, the Examiner relies on Andresen to supply this missing limitation. Again assuming, *arguendo*, that combination of Baker and Andresen is proper, that combination fails to teach or suggest all limitations recited in the independent claim 26. For example, although the unit 38 (Andresen, Figure 2) in Andresen provides an "intrinsic delay", Applicant fails to find in Andresen any discussion of the relative duration of the "intrinsic delay" of the variable delay unit 40 (Figure 2, Andresen) as compared to the intrinsic delay provided by the unit 38. In fact, Applicant fails to find any discussion in Andresen teaching that the variable delay unit 40 also has "intrinsic delay" and, if so, the size of that delay as compared to the intrinsic delay provided by the unit 38. The Examiner's reliance on Figures 5-6 in Andresen as teaching "intrinsic delays" of two sizes—one smaller and one larger

as required under claim 26—is misplaced and is not supported by the discussion of Figures 5 and 6 in Andresen at columns 6-8 therein.

Further, even though the Examiner finds Andresen combinable with Baker to reject claim 26, Applicant respectfully disagrees with that finding. Applicant observes that the Examiner doesn't point to any portion in Andresen where the desirability of combining the teachings of Andresen (e.g., output buffer 10 (including intrinsic delay unit 38 and variable delay unit 40) (Andresen, Figures 1-2)) with the teachings of Baker (e.g., a delay locked loop design) is taught or suggested.

From the above, Applicant asserts that Andresen fails to supply the larger-smaller intrinsic delay claim limitation missing from Baker, contrary to what is asserted by the Examiner. Therefore, the combined teachings of Andresen and Baker fail to teach or suggest all the claim limitations recited in the independent claim 26 and, hence, fail to render claim 26 obvious under 35 U.S.C. § 103(a). Reconsideration and allowance of claim 26 is respectfully requested.

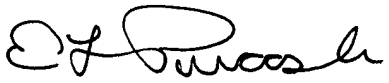
Claims 27-30 are dependent on allowable independent claim 26 and, hence, are also not rendered obvious by the combined teachings of Baker and Andresen. Therefore, reconsideration and allowance of claims 27-30 is respectfully requested.

Based on the foregoing, Applicant asserts that the Examiner has failed to establish a *prima facie* case of obviousness of claims 21-30 as required under MPEP §§ 2142, 2143 (Eighth Edition incorporating Revision No. 1, 2003) because the combination of cited prior art references Baker and Andresen fails to teach or suggest all the claim limitations in each of the claims 21-30. In view of the arguments given hereinabove, Applicant requests that the Examiner withdraw the § 103(a) rejections of pending claims 21-30.

CONCLUSION

In the present response, all rejections to the claims in the Office Action of June 22, 2004 are believed to have been addressed. Applicants therefore assert that all pending claims 1-50 are in condition for allowance and a notice by the Office to this effect is respectfully requested. If the Examiner has any questions, comments or suggestions, the undersigned Attorney earnestly requests a telephone conference at the Examiner's convenience.

Respectfully submitted,



Edward L. Pencoske
Reg. No. 29,688
Thorp Reed & Armstrong LLP
One Oxford Centre, 14th Floor
Pittsburgh, PA 15219-1425
(412) 394-7789

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Attorneys for Applicant